REMARKS

Claims 1-34 are pending in this application. By this Amendment, claims 33 and 34 are added.

In the Advisory Action, the 35 U.S.C. §101 double patenting rejection was withdrawn and the references cited with the Information Disclosure Statement filed January 13, 2005 were indicated to have been considered. It is requested that the Examiner return an initialed Form PTO-1449 indicating consideration of the references cited in that Information Disclosure Statement.

The rejection of claims 1, 6, 21 and 26-32 under 35 U.S.C. §103(a) over Kida et al. (Kida), U.S. Patent No. 6,335,728 in view of Shimamoto, U.S. Patent No. 6,147,672, claims 2-5, 7-10 and 22-25 under 35 U.S.C. §103(a) over Kida in view of Shimamoto and Chida, U.S. Patent No. 6,313,863, and claims 11-20 under 35 U.S.C. §103(a) over Kida in view of Shimamoto and Silverman et al, (Silverman), U.S. Patent No. 6,370,603 remain. The rejections are respectfully traversed.

Page 2, paragraphs 1-9, of the Advisory Action addresses some of the arguments presented in the Request for Reconsideration filed February 28, 2005. Applicant herein provides a response to the comments presented in the Advisory Action.

Paragraphs 2-4 on page 2 of the Advisory Action fail to address the issue that Kida and Shimamoto fail to disclose or suggest a RAM-incorporated driver with a first port through which still-image data or a given command is input from an external MPU and a second port through which the moving-image data, which is transferred serially over a serial transfer line from the external MPU, is input as a differential signal, as recited in claim 1.

Paragraph 2 argues that "an MPU that is external to a RAM-incorporate drive" is recited in the preamble and has thus not been given patentable weight. This is not correct because the preamble of claim 1 clearly does not recite this feature.

Paragraph 3 argues that the switches SW31, SW32 of Kida receive a data input signal from the data processing circuit 33. However, this argument does not address the issue that the data processing circuit 33 is not external to Kida's driving apparatus. The driving apparatus includes an A/D converter 31, a control circuit 32 and an image processing circuit 33 (col. 10, lines 12-25). Each of the field memories 34A, 34B has a capacity that is capable of storing at least the pixel data of one field. The field memories 34A, 34B are connected to the image data processing circuit 33 via switches SW31, SW32 which are serially connected (col. 10, lines 26-30). The switches SW31, SW32 thus fail to receive a data input signal from an external MPU because the data processing circuit 33 is internal to the driving apparatus.

Paragraph 4 argues that the teaching of Kida's references in view of the teaching of Shimamoto's reference provide and establish the "substantial evidence" to produce the features of claim 1. However, this argument and the outstanding Office Action fail to address the issue that neither Kida nor Shimamoto disclose or suggest the external MPU and thus fail to establish any motivation or suggestion to use an external MPU.

For the reasons discussed above and the Request for Reconsideration filed February 28, 2005, Kida and Shimamoto fail to disclose or suggest a RAM-incorporated driver with a first port through which still-image data or a given command is input from an external MPU and a second port through which the moving-image data, which is transferred serially over a serial transfer line from the external MPU, is input as a differential signal, as recited in claim 1.

Paragraphs 5-7 on page 2 of the Advisory Action fail to address the issue that Kida and Shimamoto fail to disclose or suggest a RAM-incorporated driver with a second port that is independent from a first port, as recited in claims 27 and 28.

Paragraph 5 argues that the feature of a second port that is independent from a first port is recited in the preamble and has thus not been given patentable weight. This is not correct because the preamble of claims 27 and 28 clearly do not recite this feature.

Paragraph 6 argues that the feature of "an MPU that is external to a RAM-incorporate driver" and "a RAM-incorporated driver with a second port that is independent from a first port" are not recited in the rejected claims. This is not correct because claim 1 clearly recites an external MPU and claims 27 and 28 clearly recite a second port that is independent from a first port.

Paragraph 7 argues that the switches SW31, SW32 are serially connected and thus controlled independently by the control circuit 32. This argument fails to address the issue that switches SW31, SW32 cannot be both serially connected and independent from each other. If the switches SW31, SW 32 are serially connected, one switch cannot be free from the influence of the other switch (i.e., they can not be independent). As clearly shown in Fig. 7 of Kida, data cannot travel from the switch SW31 to the field memories 34A, 34B without using the other switch SW32. Applicant thus adds claims 33 and 34 to further clarify this feature by reciting that the first port is not directly connected to the second port.

For the reasons discussed above and the Request for Reconsideration filed February 28, 2005, Kida and Shimamoto fail to disclose or suggest a RAM-incorporated driver with a second port that is independent from a first port, as recited in claims 27 and 28.

Paragraphs 8 and 9 on page 2 of the Advisory Action fail to address the issue that Kida and Shimamoto fail to disclose or suggest a RAM which stores the still-image data that was input through the first port and the moving-image data that was created by the reception circuit and a first control circuit and a second control circuit that operate using the RAM, as recited in claim 1 and as similarly recited in claims 27 and 28.

Paragraph 8 argues that Kida teaches a field memory 34A and a field memory 34B that store both moving image data and still image data through the switches SW31, SW32. However, this argument fails to address the issue that Kida requires two field memories 34A, 34B whereas claims 1, 27 and 28 only require a single memory (i.e., a RAM). Kida's structure is thus complicated when compared to the structure of claims 1, 27 and 28 because the control circuits of Kida operate using data stored in two separate memories rather than a single RAM, as recited in claims 1, 27 and 28.

Paragraph 9 argues that a single RAM that stores still-image data and moving-image data is not recited in claims 1, 27 and 28. This is not correct because claims 1, 27 and 28 clearly recite a RAM (i.e., a single RAM).

For the reasons discussed above and the Request for Reconsideration filed February 28, 2005, Kida and Shimamoto fail to disclose or suggest a RAM which stores the still-image data that was input through the first port and the moving-image data that was created by the reception circuit and a first control circuit and a second control circuit that operate using the RAM, as recited in claim 1 and as similarly recited in claims 27 and 28.

Chida and Silverman fail to overcome the deficiencies of Kida and Shimamoto in disclosing or suggesting all of the features recited in claims 1, 27 and 28.

In view of the foregoing, none of the applied references disclose or suggest all of the features recited in claims 1, 27 and 28 as well as the additional features recited in the dependent claims thereof. It is respectfully requested that the rejections be withdrawn.

In view of the foregoing and the Request for Reconsideration, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-34 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

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Attachments:
Petition for Extension of Time
Request for Continued Examination
Amendment Transmittal

Date: March 30, 2005

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